

What is claimed is:

1. A ferroelectric random access memory (FRAM) device comprising:
  2. a lower electrode;
  3. a lower seed layer formed on the lower electrode;
  4. a ferroelectric layer formed on the lower seed layer;
  5. an upper seed layer formed on the ferroelectric layer; and
  6. an upper electrode formed on the upper seed layer.
2. The FRAM device according to claim 1, wherein the ferroelectric layer is a PZT layer.
3. The FRAM device according to claim 1, wherein the upper and lower seed layers make characteristics of an upper interface and a lower interface of the ferroelectric match each other.
1. 4. The FRAM device according to claim 1, wherein the upper and lower seed layers are composed of a material having a crystallization temperature lower than that of a material of the ferroelectric layer.
1. 5. The FRAM device according to claim 1, wherein the upper and lower seed layers are composed of a ferroelectric material having a lattice constant similar to that of

3 a material of the ferroelectric layer.

1 6. The FRAM device according to claim 2, wherein the upper and lower seed  
2 layers are composed of  $\text{PbTiO}_3$ ,  $\text{TiO}_2$  or PZT having at least one of a higher Pb content  
3 and a higher Ti composition ratio than the PZT of the ferroelectric layer.

1 7. The FRAM device according to claim 1, wherein the upper and lower  
2 electrodes include a Pt-group metal layer, a conductive oxide layer or a dual layer of the  
3 Pt-group metal layer and the conductive oxide layer.

1 8. The FRAM device according to claim 1, further comprising:  
2 a switching element electrically connected to the lower electrode.

1 9. The FRAM device according to claim 1, further comprising:  
2 a gate insulating layer under the lower electrode;  
3 a semiconductor substrate under the gate insulating layer; and  
4 source and drain regions in a portion of the semiconductor substrate adjacent to  
5 a periphery of the gate insulating layer.

1 10. The FRAM device according to claim 6, wherein the upper and lower  
2 electrodes include of a Pt-group metal layer, a conductive oxide layer or a dual layer of

3 the Pt-group metal layer and the conductive oxide layer.

1 11. The FRAM device according to claim 1, wherein the upper and lower  
2 electrodes have the same structure.

1 12. The FRAM device according to claim 1, wherein the upper and lower seed  
2 layers are composed of the same material.

1 13. A method for fabricating a ferroelectric random access memory (FRAM)  
2 device comprising:

3 a) forming a lower electrode;  
4 b) forming a lower seed layer on the lower electrode;  
5 c) forming a ferroelectric layer on the lower seed layer;  
6 d) forming an upper seed layer on the ferroelectric layer;  
7 e) annealing a structure resulting from a)-d), including making characteristics of  
8 a lower face and an upper face of the ferroelectric layer be the same and completing a  
9 stable perovskite crystal structure of the ferroelectric layer; and  
10 f) forming an upper electrode on the upper seed layer.

1 14. The method according to claim 13, wherein forming a ferroelectric layer  
2 comprises forming a PZT ferroelectric layer on the lower seed layer.

1 15. The method according to claim 13, wherein the forming the upper and  
2 lower seed layers includes using a material having a crystallization temperature lower  
3 than that of a material for forming the ferroelectric layer.

16. The method according to claim 13, wherein the forming the upper and lower seed layers includes using a ferroelectric material having a lattice constant similar to that of a material for forming the ferroelectric layer.

17. The method according to claim 14, wherein the forming the upper and  
2 lower seed layers includes using  $PbTiO_3$ ,  $TiO_2$  or PZT having at least one of a higher Pb  
3 content and a higher Ti composition ratio than a PZT to be used to form the ferroelectric  
4 layer.

1           18.    The method according to claim 13, wherein the forming the lower electrode  
2        and the upper electrode includes using a Pt-group metal layer, a conductive oxide layer  
3        or a dual layer of the Pt-group metal layer and the conductive oxide layer.

19. The method according to claim 13, further comprising, prior to the forming of the lower electrode, forming a switching element to be electrically connected to the lower electrode.

1        20. The method according to claim 13, further comprising:  
2            before the forming the lower electrode  
3                    providing a semiconductor substrate; and  
4                    forming a gate insulating layer on the semiconductor substrate, and  
5            after the forming the upper electrode  
6                    forming source and drain regions in a portion of the semiconductor  
7                    substrate adjacent to a periphery of the gate insulating layer.

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